

ABSTRACT

5 A method and apparatus are disclosed for allocating functional units in a
 multithreaded very large instruction word (VLIW) processor. The present invention combines
 the techniques of conventional very long instruction word (VLIW) architectures and conventional
 multithreaded architectures to reduce execution time within an individual program, as well as
 across a workload. The present invention utilizes instruction packet splitting to recover some
 efficiency lost with conventional multithreaded architectures. Instruction packet splitting allows
 10 an instruction bundle to be partially issued in one cycle, with the remainder of the bundle issued
 during a subsequent cycle. The allocation hardware assigns as many instructions from each
 packet as will fit on the available functional units, rather than allocating all instructions in an
 instruction packet at one time. Those instructions that cannot be allocated to a functional unit are
 retained in a ready-to-run register. On subsequent cycles, instruction packets in which all
 15 instructions have been issued to functional units are updated from their thread's instruction
 stream, while instruction packets with instructions that have been held are retained. The
 functional unit allocation logic can then assign instructions from the newly-loaded instruction
 packets as well as instructions that were not issued from the retained instruction packets.

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